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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/520,190	01/04/2005	Josephus Arnoldus Kahlman	NL 020658	7686

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EXAMINER	
HEYI, HENOK G	

ART UNIT	PAPER NUMBER
2627	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/520,190	KAHLMAN, JOSEPHUS ARNOLDUS	
	Examiner	Art Unit	
	Henok G. Heyi	2627	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-12 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-12 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. Claims 10-12 are objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim 8. See MPEP § 608.01(n). Accordingly, the claims 10-12 not been further treated on the merits.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Buchschacher et al 6,052,295 (Buchschacher hereinafter).

Regarding claim 1, Buchschacher teaches an electronic circuit comprising conversion means (see Fig. 1 and col 1 lines65-67) for converting an input voltage (U_i, col2 line 4) into an output voltage (U_0, col 2 line 14), comprising at least a first energy storage means (a first capacitor C1, col 2 line 55) and a second energy storage means (output capacitor C_{out}, col 4 line 6) and switching means (Sw1, Sw2, Sw3, Sw4 and Sw5, Fig. 2) for periodically coupling said energy storage means (C 1, C2) to one another under the control of a clock signal so as to store energy in the energy storage means (C1, C2) and transferring at least a portion of the stored energies between the energy storage means (instead of programming the desired clock input signals the

invention also makes it possible to automatically generate the desired clock input signal. For this, monitoring means must be coupled between the output OP of the voltage converter and an input of the means, col 2 lines 31-36), characterized in that the clock signal is kept in a holding state during a holding period (R_T) during operation, which holding state is equal to the state of the clock signal immediately before the holding state (The clock signals can be programmed to a part of the voltage multiplier to a non-active state, see Abstract).

Regarding claim 2, Buchschacher teaches an electronic circuit as claimed in claim 1, characterized in that the switching means and the energy storage means are implemented with the use of at least one charge pump (CHGPMP1 - CHGPMP4, col 2 lines 45-65).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Buchschacher in view of Lenssen et al. 6,986,151 B2 (Lenssen hereinafter).

Regarding claim 3, Buchschacher teaches an integrated circuit (IC) that comprises an electronic circuit as defined in claim 1 or 2 but fails to teach a medium for storage/reading of user information, comprising an integrated circuit (IC) that comprises an electronic circuit. However, Lenssen teaches an information carrier provided with a storage unit, an integrated circuit and a coupling element (col 1 lines 4-5).
It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the electronic circuit of Buchschacher to make it usable on storage/reading medium as thought by Lenssen. The modification would have been obvious because of the benefit of storing data and energy as taught by Lenssen (col 1 line 64).

6. Claims 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buchschacher in view of Lenssen and further in view of Dierschke et al. 5,567,976 (Dierschke hereinafter).

Regarding claim 4, Buchschacher teaches providing the input voltage (Ui) from the voltage source and Lenssen teaches an information carrier provided with a storage unit, an integrated circuit and a coupling element but both Buchschacher and Lenssen fail to teach a medium as claimed in claim 3, characterized in that the integrated circuit (IC) comprises a photosensitive sensor (SNS) for providing the input voltage (Ui) when the sensor (SNS) receives a substantial quantity of light. However, the use of

photosensitive sensors in ICs is well known in the art, and as an example Dierschke teaches integrated circuits including photosensitive sensors.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the electronic circuit of Buchschacher to have a photosensitive sensor thereby to control the input voltage based on the quantity of light. The modification would have been obvious because of the benefit of photosensitive sensors not only for position sensing but also light sensing and voltage controlling.

Regarding claim 5, Lenssen teaches a medium as claimed in claim 4, characterized in that the integrated circuit (IC) furthermore comprises memory means (MM) which are provided with a supply voltage through utilization of the output voltage (one IC comprising an electrically programmable memory and the other IC a preprogrammed memory, col 3 line 40).

Regarding claim 6, Lenssen teaches a medium as claimed in claim 5, characterized in that the IC in addition comprises a microprocessor (uP), which microprocessor (uP) processes the additional information, and which microprocessor (uP) is coupled to the memory means (MM) for storing the processed additional information (the IC comprises a micro-processor by means of which algorithms can be carried out, and a memory, col 3 lines 25-27) but fails to teach a photosensitive sensor (SNSF) for providing additional information to the microprocessor (uP). However, the use of photosensitive sensors in ICs is well known in the art, and as an example Dierschke teaches integrated circuits including photosensitive sensors.

Regarding claim 7, Lenssen teaches a medium as claimed in claim 5, characterized in that the integrated circuit (IC) further comprises a microprocessor (uP), and in that the microprocessor (uP) is coupled to the memory means (MM) for processing the additional information after reading of the additional information from the memory means (the IC comprises a micro-processor by means of which algorithms can be carried out, and a memory, col 3 lines 25-27) but fails to teach a photosensitive sensor (SNSF) for providing additional information to the memory means (MM) for the storage of the additional information. However, the use of photosensitive sensors in ICs is well known in the art, and as an example Dierschke teaches integrated circuits including photosensitive sensors.

7. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buchschacher in view of Lenssen and Dierschke as applied to claim 4 above, and further in view of Arimoto et al. US 2002/0172070 A1 (Arimoto hereinafter).

Regarding claim 8, Lenssen teaches a medium as claimed in claim 6 or 7, but fails to teach that the medium is characterized in that the length of the holding period (RT) corresponds by approximation to that of a time period during which the photosensitive sensor (SNS) does not receive a substantial quantity of fight. However, Arimoto teaches even if the voltage of the storage node of the memory cell storing the H level data drops during the data holding period, the amount of outflow electric charges is sufficiently small if the capacitance of junction capacitance Cj is sufficiently small. (page 19 para [0297]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the electronic circuit of Buchschacher to have a photosensitive sensor thereby to control the input voltage based on the quantity of light. The modification would have been obvious because of the benefit of photosensitive sensors not only for position sensing but also light sensing and voltage controlling.

Regarding claim 9, a medium as claimed in claim 8, characterized in that the microprocessor (uP) is idle during the holding period (R_T), and in that the microprocessor (uP) is provided with a supply voltage from a standby circuit (SB) during the holding period (R_T).

Regarding claim 9, a medium as claimed in claim 8, characterized in that the microprocessor (uP) is idle during the holding period (Rr), and in that the microprocessor (uP) is provided with a supply voltage from a standby circuit (SB) during the holding period (R_T).

Conclusion

The referenced citations made in the rejection(s) above are intended to exemplify areas in the prior art document(s) in which the examiner believed are the most relevant to the claimed subject matter. However, it is incumbent upon the applicant to analyze the prior art document(s) in its/their entirety since other areas of the document(s) may be relied upon at a later time to substantiate examiner's rationale of record. A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. W.L. Gore & associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984). However, "the prior art's mere disclosure of more than one alternative does not constitute a teaching away from any of these alternatives because such disclosure does not criticize, discredit, or otherwise discourage the solution claimed...." In re Fulton, 391 F.3d 1195, 1201, 73 USPQ2d 1141, 1146 (Fed. Cir. 2004).

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Henok G. Heyi whose telephone number is (571) 270-1816. The examiner can normally be reached on Monday to Friday 8:30 to 6:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoa Nguyen can be reached on (571) 272-7579. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HGH
Patent Examiner
12/03/2007

TAN DINH
PRIMARY EXAMINER
12/10/07